IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Michael C. Stolowitz

Application No.: 10/822,115 Group No.: 2188
Filed: 04/08/2004 Examiner: Walter, Craig E.
For: METHOD AND APPARATUS FOR SYNCHRONIZING DATA FROM ASYNCHRONOUS DISK DRIVE DATA TRANSFERS

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION--37 C.F.R. § 41.37)

1. This brief is in furtherance of the Notice of Appeal, filed in this case on 06/26/2007, and in response to the Notice of Panel Decision from Pre-Appeal Brief Review, mailed 09/25/2007.

2. STATUS OF APPLICANT

This application is on behalf of other than a small entity.

3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 C.F.R. § 41.20(b)(2), the fee for filing the Appeal Brief is:

other than a small entity	$510.00
Appeal Brief fee due	**$510.00**

4. EXTENSION OF TERM

The proceedings herein are for a patent application and the provisions of 37 C.F.R. § 1.136 apply.

Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal brief fee	$510.00
Extension fee (if any)	$0.00
TOTAL FEE DUE	**$510.00**

6. FEE PAYMENT

Authorization is hereby made to charge the amount of $510.00 to Deposit Account No. 50-1351 (Order No. NVIDP486).

7. FEE DEFICIENCY

If any additional extension and/or fee is required, and if any additional fee for claims is required, charge Deposit Account No. 50-1351 (Order No. NVIDP486).

Date: October 25, 2007

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	
Stolowitz, Michael C.	Group Art Unit: 2188
Application No. 10/822,115	Examiner: Walter, Craig E.
Filed: 04/08/2004	Atty. Docket No. NVIDP486/P003259
For: METHOD AND APPARATUS FOR SYNCHRONIZING DATA FROM ASYNCHRONOUS DISK DRIVE DATA TRANSFERS	Date: 10/25/2007

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

APPEAL BRIEF (37 C.F.R. § 41.37)

This brief is in furtherance of the Notice of Appeal, filed in this case on 06/26/2007, and in response to the Notice of Panel Decision from Pre-Appeal Brief Review, mailed 09/25/2007.

The fees required under § 1.17, and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains these items under the following headings, and in the order set forth below (37 C.F.R. § 41.37(c)(i)):

The final page of this brief bears the practitioner's signature.

I REAL PARTY IN INTEREST (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is NVIDIA Corporation.

II RELATED APPEALS AND INTERFERENCES (37 C.F.R. § 41.37(c) (1)(ii))

With respect to other prior or pending appeals, interferences, or related judicial proceedings that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal, there are no other such appeals, interferences, or related judicial proceedings.

A Related Proceedings Appendix is appended hereto.

III STATUS OF CLAIMS (37 C.F.R. § 41.37(c) (1)(iii))

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-31

B. STATUS OF ALL THE CLAIMS IN APPLICATION

1. Claims withdrawn from consideration: None
2. Claims pending: 1-31
3. Claims allowed: None
4. Claims rejected: 1-31
5. Claims cancelled: None

C. CLAIMS ON APPEAL

The claims on appeal are: 1-31

See additional status information in the Appendix of Claims.

IV STATUS OF AMENDMENTS (37 C.F.R. § 41.37(c)(1)(iv))

As to the status of any amendment filed subsequent to final rejection, there are no such amendments after final.

V SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R. § 41.37(c)(1)(v))

With respect to a summary of Claim 1, as shown in Figures 1-4 et al., a method is provided for reading stored data from an array of independent disk drives so as to provide synchronous data transfer into a buffer. In use, for each disk drive (e.g. see items 12 and 20 of Figure 1, etc.) in the array (e.g. see item 10 of Figure 1, etc.), a corresponding two-port memory (e.g. see items 26 and 28 of Figure 1, etc.) is provided for receiving and storing read data responsive to timing signals provided by the respective drive. In addition, a READ command is initiated to each of the drives of the array, thereby causing each of the drives to retrieve selected elements of its stored data, and to transfer the retrieved data from the drive into its corresponding two-port memory using the timing signals provided by the respective drive. Further, each of the two-port memories is monitored to detect a non-empty condition. Further still, waiting is performed until all of the two-port memories indicate such a non-empty condition. Additionally, the transferred data is then synchronously read from all of the two-port memories, thereby forming synchronous read data, and the synchronous read data is written into the buffer (e.g. see items 52 of Figure 1, and item 350 of Figure 4, etc.). Furthermore, said monitoring, waiting, reading and writing into the buffer steps are repeated until completion of a read operation initiated by the said READ command. See, for example, paragraphs [0008] – [0010] et al.

With respect to a summary of Claim 10, as shown in Figures 1-4 et al., a method is provided for reading stored data from a redundant array of independent disk drives (RAID array). In use, for each disk drive (e.g. see items 12 and 20 of Figure 1, etc.) in the RAID array (e.g. see item 10 of Figure 1, etc.), a corresponding first-in first-out (FIFO) memory (e.g. see items 26 and 28 of Figure 1, etc.) arranged for receiving and storing read data using timing signals provided by the respective drive is provided. In addition, a READ command is initiated to each of the drives of the RAID array, thereby causing each of the drives to retrieve selected elements of its stored data, and the retrieved data is transferred from the drive into its corresponding FIFO memory using the timing signals provided by the respective drive. Further, each of the FIFO memories is monitored to detect a non-empty condition. Further still, waiting is performed until all of the FIFO memories indicate such a non-empty condition. Additionally, the transferred data is then synchronously read from all of the FIFO memories, thereby forming synchronous read data. Also, the synchronous read data is written into a common buffer (e.g. see items 52 of Figure 1,

and item 350 of Figure 4, etc.). Furthermore, said monitoring, waiting, reading and writing steps are repeated until completion of a read operation initiated by the READ command. See, for example, paragraphs [0008] – [0010] and [0029] et al.

With respect to a summary of Claim 17, as shown in Figures 1-4 et al., an improved redundant array of independent disk drives (RAID) disk array controller is provided. In use, the controller comprises a plurality of disk drive interfaces (e.g. see items 16 and 24 of Figures 1 and 2, etc.), where each interface is provided for attaching at least one physical disk drive (e.g. see items 12 and 20 of Figure 1, etc.). In addition, the controller comprises a corresponding two-port memory (e.g. see items 26 and 28 of Figures 1 and 2, etc.) associated with each one of the disk drive interfaces, where each two-port memory is arranged to store read data provided by its associated disk drive in a disk read operation and, conversely, to provide write data that was previously-stored in the two-port memory to its associated disk drive in a disk write operation. Further, the controller comprises a logic circuit (e.g. see item 40 of Figure 1, and item 82 of Figure 2, etc.) coupled to all of the two-port memories for detecting when all of the two-port memories have data stored therein for a read operation or available space therein for a write operation. Further still, the controller comprises control circuitry (e.g. see item 50 of Figure 1, etc.) responsive to the logic circuit for synchronously reading data from all of the two-port memories only when all of the two-port memories have data stored therein, thereby forming synchronous read data. Additionally, the control circuitry is further responsive to the logic circuit for detecting that all of the two-port memories have space therein and synchronously writing data to all of the two port memories thereby forming synchronous write data. Furthermore, the controller comprises first redundant data circuitry (e.g. see item 394 of Figure 4, etc.) for regenerating missing data "on the fly" from the synchronous read data in the event that one of the disk drives fails to provide read data to its associated two-port memory in a read operation. In addition, the controller comprises second redundant data circuitry (e.g. see item 360 of Figure 3, etc.) for generating redundant data "on the fly" from the synchronous write data for storing in the array (e.g. see item 300 of Figure 3, etc.). Further, one of the disk drive interfaces is designated for connection to a redundant disk drive for storing redundant data so that the synchronous read data includes redundant data. Further still, the first redundant data circuitry for regenerating missing data is coupled to all of the two-port memories to receive the synchronous read data, including the redundant data, and further is arranged to compute a redundant data operation across the synchronous read data so as

to provide corrected data in the event of a failed drive without delaying output of the read data. See, for example, paragraphs [0008] – [0011] and [0029] et al.

With respect to a summary of Claim 26, as shown in Figures 1-4 et al., a method of writing data into an array of independent disk drives is provided. In use, a buffer (e.g. see items 52 of Figure 2, and item 350 of Figure 3, etc.) is provided for storing write data. Additionally, a corresponding two-port memory (e.g. see items 26 and 28 of Figure 2, etc.) is provided for receiving and storing write data for each disk drive (e.g. see items 12 and 20 of Figure 2, etc.) in the array (e.g. see item 10 of Figure 2, etc.). Further, each of the two-port memories is monitored to detect a non-full condition. Further still, waiting is performed until all of the two-port memories indicate such a non-full condition. In addition, write data is then read from the buffer. Furthermore, redundant data is computed from said write data. Also, the write data and the computed redundant data are synchronously stored into the two-port memories via a first port of each two-port memory. Additionally, while synchronously storing the write data and the computed redundant data into the two-port memories, stored data is transferred from a second port of each of the two-port memories into its corresponding disk drive, and in each case the previously-stored data is transferred responsive to timing control provided by the corresponding disk drive. See, for example, paragraphs [0008] – [0009] and [0011] et al.

Of course, the above citations are merely examples of the above claim language and should not be construed as limiting in any manner.

VI GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. § 41.37(c)(1)(vi))

Following, under each issue listed, is a concise statement setting forth the corresponding ground of rejection.

Issue # 1: The Examiner has rejected Claim 31 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

Issue # 2: The Examiner has rejected Claims 12 and 17-25 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which appellant regards as the invention.

Issue # 3: The Examiner has rejected Claims 1, 3-5, 8, 10-12, 14, 16, 26-28, and 31 under 35 U.S.C. 102(b) as being anticipated by Searby (U.S. Patent No. 5,765,186).

Issue # 4: The Examiner has rejected Claim 15 under 35 U.S.C. 103(a) as being unpatentable over Searby (U.S. Patent No. 5,765,186).

Issue # 5: The Examiner has rejected Claims 6, 7, 13, 29, and 30 under 35 U.S.C. 103(a) as being unpatentable over Searby (U.S. Patent No. 5,765,186), in view of Anderson (U.S. Patent Publication No. 2003/0200478 A1).

Issue # 6: The Examiner has rejected Claims 2, 9, 17, and 19-25 under 35 U.S.C. 103(a) as being unpatentable over Searby (U.S. Patent No. 5,765,186), in view of Stolowitz (U.S. Patent No. 6,018,778).

Issue # 7: The Examiner has rejected Claim 18 under 35 U.S.C. 103(a) as being unpatentable over Searby (U.S. Patent No. 5,765,186), in view of Stolowitz (U.S. Patent No. 6,018,778), and further in view of Yamamoto (U.S. Patent No. 5,801,859).

VII ARGUMENT (37 C.F.R. § 41.37(c)(1)(vii))

The claims of the groups noted below do not stand or fall together. In the present section, appellant explains why the claims of each group are believed to be separately patentable.

Issue # 1:

The Examiner has rejected Claim 31 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

Group #1: Claim 31

In the Office Action dated 03/26/2007, the Examiner has argued that 'one of ordinary skill in the art would not understand how an asserted signal (i.e. strobe) itself can be "coupled to [a memory]"' and that "one skilled in the art would recognize that only a physical medium itself, carrying said signal could be coupled to the memory." Appellant respectfully disagrees and asserts that "asserting a common write strobe coupled to all of the FIFO memories" does in fact comply with the enablement requirement.

Issue # 2:

The Examiner has rejected Claims 12 and 17-25 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which appellant regards as the invention.

Group #1: Claims 12 and 17-25

In the Office Action dated 03/26/2007, the Examiner has argued that 'the phrase "on the fly" renders the claim indefinite.' Appellant respectfully disagrees and notes that the above claim language is to be read according to the plain and ordinary meaning thereof, in view of relevant dictionary definitions, and in further view of the definitions provided in the specification.

More specifically, the phrase "on the fly" is explained in the specification (for example, see FIG. 3 "On-the-fly XOR -- Write Direction" and FIG. 4 "On-the-fly XOR -- Read Direction" and the corresponding portions of the specification. In addition, appellant notes that Paragraph [0007] of the Specification incorporates US Pat. No. 6,237,052 by reference, which discusses the phrase "on-the-fly" in detail. Such incorporation by reference was used here to reduce duplication of prior art.

Issue # 3:

The Examiner has rejected Claims 1, 3-5, 8, 10-12, 14, 16, 26-28, and 31 under 35 U.S.C. 102(b) as being anticipated by Searby (U.S. Patent No. 5,765,186).

Group #1: Claims 1, 3-5, 8, 10-12, 14, and 16

With respect to independent Claims 1 and 10, the Examiner has relied on Col. 3, lines 52-67 from the Searby reference to make a prior art showing of appellant's claimed "memory for receiving and storing read data responsive to timing signals provided by the respective drive" (see this or similar, but not necessarily identical language in the aforementioned claims).

Appellant respectfully notes that Searby discloses that "[t]he controller 51 is arranged to utilise the buffering provided by the SCSI interface and to wait until all twenty of the second interfaces have output a request signal before outputting a write strobe signal over line 54 to the RAM buffers 37 to 40" (Col. 6, line 64 – Col. 7, line 1). In addition, Searby teaches that "[w]hen data is ready for transfer a signal is sent from the interfaces 33 to 36" and that "once the controller has received signals from each of the interfaces it enables data to be transferred between the interfaces and respective RAM buffers" (Abstract).

However, waiting until all of the disc interfaces have data ready before transferring data, as in Searby, does not teach "receiving and storing read data responsive to timing signals provided by the respective drive" (emphasis added), as claimed by appellant. Additionally, "wait[ing] until all... of the second interfaces have output a request signal before outputting a write strobe

signal" (emphasis added), as in Searby, fails to disclose "receiving and storing read data responsive to timing signals provided by the respective **drive**" (emphasis added), as claimed.

In the Office Action dated 03/26/2007, the Examiner has argued that "[appellant] does in fact describe synchronizing the data transfer from drives to the buffer," and has further argued that "[appellant] concedes by his own admission that Searby synchronizes data transfer from the drives to the RAM buffer, as similarly recited by [appellant] in the preamble."

Appellant respectfully disagrees and notes that appellant claims "memory for receiving and storing read data responsive to timing signals provided by the respective drive" and "synchronously reading the transferred data from all of the...memories, thereby forming synchronous read data, and writing the synchronous read data into the buffer" (see the same or similar, but not necessarily identical language in independent Claims 1 and 10 - emphasis added), in the context claimed. Thus, Searby's mere disclosure of waiting until all of the disc interfaces have data ready before transferring data fails to meet appellant's specific claim language, namely "memory for receiving read data responsive to timing signals provided by the respective drive" in addition to "synchronously reading the transferred data from all of the...memories" (emphasis added), in the context claimed.

In addition, the excerpts relied on by the Examiner merely teach "transferring means comprising means for providing an indication when said data is available for transfer" and that "the controlling means [are] responsive to said indication from said transferring means" (Col. 3, line 59 – Col. 4, line 1 – emphasis added). However, merely disclosing controlling means responsive to an indication from a transferring means that data is available for transfer, as in Searby, does not teach "receiving and storing read data responsive to timing signals provided by the respective drive" (emphasis added), as claimed by appellant. Clearly, an indication from transferring means that data is available for transfer, as in Searby, simply fails to even suggest "timing signals provided by the respective drive" (emphasis added), in the manner as claimed by appellant.

In addition, with respect to independent Claims 1 and 10, the Examiner has relied on Col. 5, lines 38-49 from the Searby reference to make a prior art showing of appellant's claimed "causing each of the drives to... transfer the retrieved data from the drive into its corresponding two-port

memory using the timing signals provided by the respective drive" (see this or similar, but not necessarily identical language in the aforementioned claims).

Appellant again notes that merely waiting until all of the disc interfaces have data ready before transferring data, as in Searby, does not teach "transfer[ring] the retrieved data from the drive into its corresponding two-port memory using the timing signals provided by the respective drive" (emphasis added), as claimed by appellant. Additionally, "wait[ing] until all... of the second interfaces have output a request signal before outputting a write strobe signal" (emphasis added), as in Searby, fails to disclose "causing each of the drives to... transfer the retrieved data from the drive into its corresponding two-port memory using the timing signals provided by the respective **drive**" (emphasis added), as claimed.

In the Office Action dated 03/26/2007, the Examiner has argued that in "Searby in Fig. 2, and col. 5, lines 39-49, a request signal is associated with each respective drive, in order to control the transfer of information." Appellant respectfully disagrees and notes that the excerpts relied on by the Examiner merely teach that "a system controller... receives frame request data from an external processing apparatus... via request bus 52 and in response thereto outputs control data" (Col. 5, lines 39-42 – emphasis added). In addition, Searby teaches that "[t]he controller 51 also receives request signals REQ from each of the second SCSI interfaces... associated with the RAM buffers... thereby controlling the outputting of data" (Col. 5, lines 44-49 – emphasis added). However, receiving request signals which control the output of data, as in Searby, does not teach "causing each of the drives to... transfer the retrieved data from the drive into its corresponding two-port memory using the **timing signals** provided by the **respective drive**" (emphasis added), as claimed by appellant. Clearly, receiving request signals from each of the second SCSI interfaces, as in Searby, simply fails to even suggest "timing signals provided by the respective drive" (emphasis added), in the manner as claimed by appellant.

Further, with respect to independent Claims 1 and 10, the Examiner has relied on Fig. 2, element 49 and Col. 7, lines 32-46 from the Searby reference to make a prior art showing of appellant's claimed "monitoring each of the two-port memories to detect a non-empty condition" (see this or similar, but not necessarily identical language in the aforementioned claims).

More specifically, in the Office Action dated 07/13/2006, the Examiner argued that Searby "transfers the data to the data highway...based on the determination that data is stored in the RAM buffers." Further, the Examiner argued that "[s]ince all the buffers receive data substantially concurrently (i.e., all disk stores send data to the RAM buffers at the same time, which causes either all the buffers to contain data, or no buffers to contain data), each RAM is monitored to determine that data is either present (i.e., non-empty condition), or not present." In addition, the Examiner argued that "[d]ata present in the RAM buffers is an implied acknowledgement that data have been received from the disk stores" and that "the system cannot transfer data to the highway until data is present in the RAM buffers; therefore the memories are monitored for this determination to occur."

Appellant disagrees and again respectfully notes that Searby discloses that "[t]he controller 51 is arranged to utilise the buffering provided by the SCSI interface and to wait until all twenty of the second interfaces have output a request signal before outputting a write strobe signal over line 54 to the RAM buffers 37 to 40" (Col. 6, line 64 – Col. 7, line 1). Further, Searby teaches that "[a]t the same time, the controller 51 outputs RAM address data to the RAM buffers 37 to 40 so that the data from the second SCSI interfaces 33 to 36 is stored at the same respective locations in the RAM buffers 37 to 40" (Col. 6, lines 3-7).

However, merely writing data into all of the RAM buffers using a common strobe signal, in addition to providing RAM addressing, as taught in Searby, fails to disclose "monitoring <u>each</u> of the two-port memories to detect a non-empty condition" (emphasis added), as claimed by appellant. More specifically, because the controller in Searby itself effects the writes to the RAM buffers, it "knows" when they have received data from the drives. Further, as all of the RAMs receive data concurrently, monitoring any one of them would suffice to determine its status. Since the process in Searby is all synchronous, the controller has no need to "monito[r] <u>each</u> of the two-port memories to detect a non-empty condition" (emphasis added), as claimed.

In the Office Action dated 03/26/2007, the Examiner has relied on an inherency argument regarding appellant's claimed "monitoring each of the two-port memories to detect a non-empty condition," as claimed. Specifically, the Examiner has argued that "memory monitoring to some degree is inherent in a system such as Searby's." because" "Searby's system is directed to the

parallel transfer of data, [such that] the system must wait until each of the memories has data present before the data can be sent to the highway." The Examiner has thus concluded that, "[Searby's] system must inherently perform some sort of monitoring process of the memories to determine if data is present to transfer."

Appellant respectfully disagrees and asserts that Searby merely discloses that "[t]he registers 41 to 44 each hold a single word of data and the word is output therefrom as each of the tri-state buffers 45 to 48 is enabled in sequence" and that "[e]ach tri-state buffer 45 to 48 is enabled individually for output of the data word from the respective register to the highway 49" (Col. 7, lines 39-42 – emphasis added). However, merely enabling a tri-state buffer for output of the data word from the respective register, as in Searby, simply fails to even suggest "monitoring each of the two-port memories to detect a non-empty condition" (emphasis added), as claimed. In view of the arguments made hereinabove, any such inherency argument has been adequately rebutted, and a notice of allowance or a specific prior art showing of such claim features, in combination with the remaining claim elements is respectfully requested. (See MPEP 2112)

Additionally, in response, appellant asserts that the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

Further, with respect to independent Claims 1 and 10, the Examiner has relied on Fig. 2, elements 49 and 50; Col. 5, lines 22-37; Col. 6, lines 14-31; and Col. 7, lines 32-46 from the Searby reference to make a prior art showing of appellant's claimed "synchronously reading the transferred data from all of the two-port memories, thereby forming synchronous read data, and writing the synchronous read data into the buffer" (see this or similar, but not necessarily identical language in the aforementioned claims).

Appellant respectfully notes that Searby discloses that "[o]nce all of the data for the requested frame has been transferred to the RAM buffers 37 to 40 it can be output therefrom to the highway 49" and that "[d]ata is output from the RAM buffers 37 to 40 by applying a read strobe signal to the line 54 while simultaneously addressing the same location in each of the stores" (Col. 7, lines 32-37). In addition, as mentioned above, Searby teaches that "the controller 51 outputs RAM address data to the RAM buffers 37 to 40 so that the data from the second SCSI interfaces 33 to 36 is stored at the same respective locations in the RAM buffers 37 to 40" (Col. 6, lines 3-7). However, merely waiting to collect a full frame of data, where the data was already synchronized as it was written into the RAM buffer, as noted above, fails to disclose "synchronously reading the transferred data from all of the two-port memories, thereby forming synchronous read data, and writing the synchronous read data into the buffer" (emphasis added), as claimed by appellant.

In the Office Action dated 03/26/2007, the Examiner has argued that "synchronous data is formed and written at least by the time it is transmitted, hence Searby does in fact [teach] 'synchronously reading the transferred data from all of the two-port memories'" and that "therefore the data *formed* from this transmission is in fact synchronous as required by the instant claim." Appellant respectfully disagrees and notes that the excerpts from Searby relied on by the Examiner merely teach that "[o]nce all of the data for the requested frame has been transferred to the RAM buffers... it can be output therefrom to the highway" (Col. 7, lines 32-34) where "the word is output therefrom as each of the tri-state buffers 45 to 48 is enabled in sequence" and that "[e]ach tri-state buffer 45 to 48 is enabled individually for output of the data word from the respective register to the highway 49" (Col. 7, lines 40-42 – emphasis added). However, the mere disclosure that the word is output as each tri-state buffer is enabled in sequence and individually output from the register to the highway, as in Searby, simply fails to even suggest "forming synchronous read data" by "synchronously reading the transferred data from all of the two-port memories" (emphasis added), as claimed by appellant.

The Examiner is reminded that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed.

Cir. 1987). Moreover, the identical invention must be shown in as complete detail as contained in the claim. *Richardson v. Suzuki Motor Co.*868 F.2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim.

This criterion has simply not been met by the above reference, as noted above.

Group #2: Claims 26-28, and 31

With respect to independent Claim 26, the Examiner has relied on Fig. 2, element 49 and Col. 7, lines 32-46 from the Searby reference to make a prior art showing of appellant's claimed "monitoring each of the two-port memories to detect a non-full condition."

Appellant respectfully notes that the excerpts from Searby relied on by the Examiner merely teach that "[o]nce all of the data for the requested frame has been transferred to the RAM buffers... it can be output therefrom to the highway" (Col. 7, lines 32-34). However, merely teaching that data for a requested frame is output from the RAM buffers once its has all been transferred, as in Searby, does not teach "monitoring each of the two-port memories to detect a **non-full** condition" (emphasis added), as claimed by appellant.

Again, the foregoing anticipation criterion has simply not been met by the above reference, as noted above.

Issue # 4:

The Examiner has rejected Claim 15 under 35 U.S.C. 103(a) as being unpatentable over Searby (U.S. Patent No. 5,765,186).

Group #1: Claim 15

In the Office Action dated 03/26/2007, the Examiner has admitted that "Searby does not explicitly teach a method of reading data from an array... wherein each synchronous transfer of read data into the common buffer stores 64-bits of read data," but has argued that "such a

limitation is merely a matter of design choice and would have been obvious in the system of Searby." The Examiner has further admitted that "Searby teaches his register (Fig. 2, element 50) as storing information [in] 8-bit format rather than [in] 64-bit as claimed by [appellant]," but has argued that "[t]he fact that Searby differs [from] the claimed invention only by the width of the data stored fails to define a patentably distinct invention over Searby, since both the claimed invention and Searby's teachings are both directed [to] synchronous data transfer[s] from asynchronous devices."

Appellant respectfully disagrees and notes that Searby merely discloses that "[d]ata on the highway 49 is in the form of 16-bit words and is reduced to 8-bit bytes of data by a register 50 before being output from the apparatus for display or processing by an editing or a processing system" (Col. 5, lines 33-37). Further, Searby discloses that "[d]ata is transferred along the SCSI highway a byte (8 bits) at a time" and that "[e]ach second SCSI interface 33 to 36 waits until it has received a word (two bytes) of data and then outputs a request signal REQ to the controller 51" (Col. 6, lines 31-34). Further still, Searby teaches that "[i]ncoming 16-bit words of data from the register 50 are input to the parity generator 55 where they are sequentially processed in an exclusive-or operation to produce a 16-bit parity word" (Col. 9, lines 5-8). Appellant respectfully asserts that the disclosure in Searby that a register reduces <u>16-bit words</u> to <u>8-bit portions</u>, that data is transferred <u>8 bits</u> at a time, that request signals are generated after <u>2 bytes</u> of data are received, and that <u>16-bit</u> words are processed clearly demonstrates that it would <u>not</u> be obvious that "each synchronous transfer of read data into the common buffer stores <u>64-bits</u> of read data" (emphasis added), as claimed by appellant.

It thus appears that with respect to dependent Claim 15, the Examiner has simply dismissed the same under Official Notice. Appellant respectfully disagrees for the aforementioned reasons, and formally requests a specific showing of the subject matter in ALL of the claims in any future action. Note excerpt from MPEP below.

"If the [appellant] traverses such an [Official Notice] assertion the examiner should cite a reference in support of his or her position." See MPEP 2144.03.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on [appellant's] disclosure. *In re Vaeck*,947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

Appellant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art references, as relied upon by the Examiner, fail to teach or suggest <u>all</u> of the claim limitations, as noted above.

<u>Issue # 5:</u>

The Examiner has rejected Claims 6, 7, 13, 29, and 30 under 35 U.S.C. 103(a) as being unpatentable over Searby (U.S. Patent No. 5,765,186), in view of Anderson (U.S. Patent Publication No. 2003/0200478 A1).

Group #1: Claims 6, 7, and 13

Appellant respectfully asserts that such claims are not met by the prior art for the reasons argued with respect to Issue #3, Group #1.

Group #1: Claims 29 and 30

Appellant respectfully asserts that such claims are not met by the prior art for the reasons argued with respect to Issue #3, Group #2.

<u>Issue # 6:</u>

The Examiner has rejected Claims 2, 9, 17, and 19-25 under 35 U.S.C. 103(a) as being unpatentable over Searby (U.S. Patent No. 5,765,186), in view of Stolowitz (U.S. Patent No. 6,018,778).

Group #1: Claims 2 and 9

Appellant respectfully asserts that such claims are not met by the prior art for the reasons argued with respect to Issue #3, Group #1.

Group #2: Claims 17 and 19-25

Further, with respect to independent Claim 17, the Examiner has relied on Fig. 2, elements 49 and 50; Col. 5, lines 22-37; Col. 6, lines 14-31; and Col. 7, lines 32-46 from the Searby reference to make a prior art showing of appellant's claimed "synchronously reading data from all of the two-port memories only when all of the two-port memories have data stored therein, thereby forming synchronous read data."

Appellant respectfully notes that Searby discloses that "[o]nce all of the data for the requested frame has been transferred to the RAM buffers 37 to 40 it can be output therefrom to the highway 49" and that "[d]ata is output from the RAM buffers 37 to 40 by applying a read strobe signal to the line 54 while simultaneously addressing the same location in each of the stores" (Col. 7, lines 32-37). In addition, as mentioned above, Searby teaches that "the controller 51 outputs RAM address data to the RAM buffers 37 to 40 so that the data from the second SCSI interfaces 33 to 36 is stored at the same respective locations in the RAM buffers 37 to 40" (Col. 6, lines 3-7). However, merely waiting to collect a full frame of video data, where the data was already synchronized as it was written into the RAM buffer, fails to disclose "<u>synchronously reading</u> data <u>from all of the two-port memories</u>...thereby <u>forming synchronous read data</u>" (emphasis added), as claimed by appellant.

In the Office Action dated 03/26/2007, the Examiner has argued that "synchronous data is formed and written at least by the time it is transmitted, hence Searby does in fact [teach] 'synchronously reading the transferred data from all of the two-port memories'" and that

"therefore the data *formed* from this transmission is in fact synchronous as required by the instant claim." Appellant respectfully disagrees and notes that the excerpts from Searby relied on by the Examiner merely teach that "[o]nce all of the data for the requested frame has been transferred to the RAM buffers... it can be output therefrom to the highway" (Col. 7, lines 32-34) where "the word is output therefrom as each of the tri-state buffers 45 to 48 is enabled in sequence" and that "[e]ach tri-state buffer 45 to 48 is enabled individually for output of the data word from the respective register to the highway 49" (Col. 7, lines 40-42 – emphasis added). However, the mere disclosure that the word is output as each tri-state buffer is enabled in sequence and individually output from the register to the highway, as in Searby, simply fails to even suggest "forming synchronous read data" by "synchronously reading data from all of the two-port memories" (emphasis added), as claimed by appellant.

Appellant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art references, as relied upon by the Examiner, fail to teach or suggest all of the claim limitations, as noted above.

Issue # 7:

The Examiner has rejected Claim 18 under 35 U.S.C. 103(a) as being unpatentable over Searby (U.S. Patent No. 5,765,186), in view of Stolowitz (U.S. Patent No. 6,018,778), and further in view of Yamamoto (U.S. Patent No. 5,801,859).

Group #1: Claim 18

Appellant respectfully asserts that such claims are not met by the prior art for the reasons argued with respect to Issue #6, Group #2.

In view of the remarks set forth hereinabove, all of the independent claims are deemed allowable, along with any claims depending therefrom.

VIII CLAIMS APPENDIX (37 C.F.R. § 41.37(c)(1)(viii))

The text of the claims involved in the appeal (along with associated status information) is set forth below:

1. (Previously Presented) A method of reading stored data from an array of independent disk drives so as to provide synchronous data transfer into a buffer, the method comprising:

for each disk drive in the array, providing a corresponding two-port memory for receiving and storing read data responsive to timing signals provided by the respective drive;

initiating a READ command to each of the drives of the array, thereby causing each of the drives to retrieve selected elements of its stored data, and to transfer the retrieved data from the drive into its corresponding two-port memory using the timing signals provided by the respective drive;

monitoring each of the two-port memories to detect a non-empty condition;

waiting until all of the two-port memories indicate such a non-empty condition;

then synchronously reading the transferred data from all of the two-port memories, thereby forming synchronous read data, and writing the synchronous read data into the buffer; and

repeating said monitoring, waiting; reading and writing into the buffer steps until completion of a read operation initiated by the said READ command.

2. (Previously Presented) A method of reading stored data according to claim 1 wherein:

the transferred data includes user data as well as redundant data sufficient to enable reconstruction of all of the user data in the event of a failure of any single drive of the array and the method further comprising,

in the event that one of the disk drives fails, executing said initiating, monitoring, waiting and synchronously reading steps only with respect to the non-failed drives; and dynamically regenerating missing data corresponding to the failed drive from the synchronous read data.

3. (Previously Presented) A method of reading stored data from an array according to claim 1 wherein each two-port memory comprises a first-in first-out (FIFO) memory.

4. (Previously Presented) A method of reading stored data from an array according to claim 3 wherein the array comprises a redundant array.

5. (Previously Presented) A method of reading stored data from an array according to claim 4 and further comprising, in the event that one of the disk drives of the redundant array has failed , dynamically regenerating missing data corresponding to the failed drive from the synchronous read data.

6. (Previously Presented) A method of reading stored data from an array according to claim 1 wherein at least one of the disk drives is coupled to its corresponding two-port memory via an Ultra-DMA (UDMA) interface.

7. (Previously Presented) A method of reading data from an array according to claim 1 wherein the read operation is effected via a corresponding Ultra-DMA (UDMA) interface to each of the disk drives.

8. (Previously Presented) A method of reading data from an array according to claim 1 wherein said synchronously reading the stored data from all of the two-port memories comprises asserting a common read enable signal to each of the memories.

9. (Previously Presented) A method of reading data from an array according to claim 1 wherein said synchronously reading the stored data from all of the two-port memories is conducted over a single direct memory access (DMA) channel.

10. (Previously Presented) A method of reading stored data from a redundant array of independent disk drives (RAID array) comprising:

for each disk drive in the RAID array, providing a corresponding first-in first-out (FIFO) memory arranged for receiving and storing read data using timing signals provided by the respective drive;

initiating a READ command to each of the drives of the RAID array, thereby causing each of the drives to retrieve selected elements of its stored data, and to transfer the retrieved

data from the drive into its corresponding FIFO memory using the timing signals provided by the respective drive;

monitoring each of the FIFO memories to detect a non-empty condition;

waiting until all of the FIFO memories indicate such a non-empty condition;

then synchronously reading the transferred data from all of the FIFO memories, thereby forming synchronous read data;

writing the synchronous read data into a common buffer; and

repeating said monitoring, waiting, reading and writing steps until completion of a read operation initiated by the READ command.

11. (Previously Presented) A method of reading stored data according to claim 10 wherein the stored data is word striped over the redundant array.

12. (Previously Presented) A method of reading stored data according to claim 10 and further comprising, in the event that one of the disk drives fails to transfer read data to its associated FIFO memory, regenerating the missing read data "on the fly" from the synchronous read data.

13. (Previously Presented) A method of reading data according to claim 10 wherein each of the drives is coupled to its associated FIFO memory via a Ultra-DMA (UDMA) interface.

14. (Original) A method of reading data according to claim 10 wherein the synchronous transfer of read data into the common buffer is implemented with a single address counter and a common FIFO read enable signal.

15. (Original) A method of reading data from an array according to claim 10 wherein each synchronous transfer of read data into the common buffer stores 64-bits of read data.

16. (Original) A method of reading data from an array according to claim 10 and further comprising providing a FIFO memory in the data path between the individual drive FIFO memories and the common buffer.

17. (Previously Presented) An improved redundant array of independent disk drives (RAID) disk array controller comprising:

a plurality of disk drive interfaces, each interface for attaching at least one physical disk drive;

a corresponding two-port memory associated with each one of the disk drive interfaces, each two-port memory arranged to store read data provided by its associated disk drive in a disk read operation and, conversely, to provide write data that was previously-stored in the two-port memory to its associated disk drive in a disk write operation;

a logic circuit coupled to all of the two-port memories for detecting when all of the two-port memories have data stored therein for a read operation or available space therein for a write operation;

control circuitry responsive to the logic circuit for synchronously reading data from all of the two-port memories only when all of the two-port memories have data stored therein, thereby forming synchronous read data;

the control circuitry further responsive to the logic circuit for detecting that all of the two-port memories have space therein and synchronously writing data to all of the two port memories thereby forming synchronous write data;

first redundant data circuitry for regenerating missing data "on the fly" from the synchronous read data in the event that one of the disk drives fails to provide read data to its associated two-port memory in a read operation; and

second redundant data circuitry for generating redundant data "on the fly" from the synchronous write data for storing in the array

and wherein:

one of the disk drive interfaces is designated for connection to a redundant disk drive for storing redundant data so that the synchronous read data includes redundant data;

the first redundant data circuitry for regenerating missing data is coupled to all of the two-port memories to receive the synchronous read data, including the redundant data, and further is arranged to compute a redundant data operation across the synchronous read data so as to provide corrected data in the event of a failed drive without delaying output of the read data.

18. (Original) An improved RAID disk array controller according to claim 17 and wherein each two-port memory has multiplexers for exchanging its input and output ports depending on the

data transfer direction.

19. (Previously Presented) An improved RAID disk array controller according to claim 17 wherein each two-port memory comprises a first-in first-out (FIFO) memory.

20. (Previously Presented) An improved RAID disk array controller according to claim 17 wherein the common buffer comprises dynamic random-access memory (DRAM).

21. (Previously Presented) An improved RAID disk array controller according to claim 17 and further comprising a single address counter arranged for addressing the buffer for transfers between the buffer and the first-in first-out (FIFO) memories in either direction.

22. (Previously Presented) An improved disk array controller according to claim 17 wherein at least one disk drive interface implements a AT Attachment and ATA Packet Interface (ATA/ATAPI) protocol.

23. (Previously Presented) An improved disk array controller according to claim 17 wherein all of the disk drive interfaces implement a AT Attachment and ATA Packet Interface (ATA/ATAPI) protocol.

24. (Original) An improved disk array controller according to claim 17, implemented on a motherboard.

25. (Original) An improved disk array controller according to claim 17, implemented on a Host Bus Adapter.

26. (Previously Presented) A method of writing data into an array of independent disk drives, the method comprising:

providing a buffer for storing write data;

for each disk drive in the array, providing a corresponding two-port memory for receiving and storing write data;

monitoring each of the two-port memories to detect a non-full condition;

waiting until all of the two-port memories indicate such a non-full condition;

then reading write data from the buffer;

computing redundant data from said write data;

synchronously storing the write data and the computed redundant data into the two-port memories via a first port of each two-port memory; and

while synchronously storing the write data and the computed redundant data into the two-port memories, transferring stored data from a second port of each of the two-port memories into its corresponding disk drive, in each case transferring the previously-stored data responsive to timing control provided by the corresponding disk drive.

27. (Previously Presented) A method of writing data into an array according to claim 26 and further comprising stalling said storing step whenever any of the two-port memories become full, but only with regard to the full memory, while allowing said synchronously storing the write data to continue into the non-full two-port memories.

28. (Previously Presented) A method of writing data into an array according to claim 27 wherein each two-port memory comprises a first-in first-out (FIFO) memory.

29. (Previously Presented) A method of writing data into an array according to claim 28 wherein the array includes a UDMA interface to at least one of the disk drives.

30. (Original) A method of storing data into an array according to claim 28 wherein the write operation is effected via a corresponding UDMA interface to each of the disk drives.

31. (Previously Presented) A method of storing data into an array according to claim 28 wherein said synchronously storing the write data comprises asserting a common write strobe coupled to all of the FIFO memories.

IX EVIDENCE APPENDIX (37 C.F.R. § 41.37(c)(1)(ix))

There is no such evidence.

X RELATED PROCEEDING APPENDIX (37 C.F.R. § 41.37(c)(1)(x))

N/A

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 971-2573. For payment of any additional fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP486).

Respectfully submitted,

By: /KEVINZILKA/ Date: October 25, 2007

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